

What is claimed is:

1. A method forming self-aligned contacts, comprising the steps of:
  2. forming gate stacks in a series of parallel stripes on a semiconductor
  3. substrate;
  4. forming gate spacers on the sidewalls of the gate stacks;
  5. forming conductive film pads to serve as buried contact pads between the
  6. gate spacers;
  7. forming a first interlayer insulation layer over the conductive film pads and the
  8. gate stacks;
  9. forming bit line stacks, in a series of parallel stripes skewed relative to the
  10. gate stacks, on the first interlayer insulation layer;
  11. forming bit line spacers on the sidewalls of the bit line stacks;
  12. forming a second interlayer insulation layer on the first interlayer insulation
  13. layer in such a way that upper surfaces of the bit line stacks are exposed;
  14. forming a photoresist film pattern, on the second interlayer insulation layer, in
  15. the form of laterally spaced apart stripes of photoresist extending parallel to the gate
  16. stacks, the photoresist film pattern exposing segments of the bit line stacks and
  17. exposing portions of the second interlayer insulation layer located directly above
  18. respective ones of the conductive film pads, respectively;
  19. etching the second interlayer insulation layer and the first interlayer insulation
  20. layer using the photoresist film pattern, the bit line stacks and the bit line spacers as
  21. etching masks to form contact holes exposing the conductive film pads by; and
  22. filling the contact holes with a conductive material to form conductive plugs
  23. contacting the conductive film pads.

1        2.     The method of claim 1, wherein said forming of the gate stacks  
2     comprises sequentially forming a gate insulation layer, a gate conductive layer and a  
3     gate capping layer on the semiconductor substrate.

1        3.     The method of claim 1, wherein said forming of the bit line stacks  
2     comprises sequentially forming a barrier metal layer, a bit line conductive layer and a  
3     bit line capping layer on said first interlayer insulation layer.

4        4.     The method of claim 1, wherein said forming of the second interlayer  
5     insulation layer comprises forming a layer of insulation over the first interlayer  
6     insulation layer and the bit line stacks, and planarizing said layer of insulation until  
7     the upper surfaces of said bit line stacks are exposed.

1        5.     The method of claim 4, wherein said planarizing comprises chemical  
2     mechanical polishing.

1        6.     The method of claim 1, wherein said forming of the conductive plugs  
2     comprises depositing conductive material sufficient to form a layer that fills the  
3     contact holes and covers the bit line stacks, and planarizing the layer of conductive  
4     material to expose the upper surfaces of the bit line stacks.

1        7.     The method of claim 6, wherein said planarizing comprises an etch  
2     back technique.

1        8.     The method of claim 6, wherein said planarizing comprises chemical  
2     mechanical polishing.

1           9. A method of forming a semiconductor device, comprising the steps of:  
2           forming gate stacks in a series of parallel stripes on a semiconductor  
3           substrate;  
4           forming gate spacers on the sidewalls of the gate stacks;  
5           forming conductive film pads to serve as buried contact pads between the  
6           gate spacers;  
7           forming a first interlayer insulation layer over the conductive film pads and the  
8           gate stacks;  
9           forming bit line stacks, in a series of parallel stripes skewed relative to the  
10          gate stacks, on the first interlayer insulation layer;  
11          forming bit line spacers on the sidewalls of the bit line stacks;  
12          forming a second interlayer insulation layer on the first interlayer insulation  
13          layer in such a way that upper surfaces of the bit line stacks are exposed;  
14          forming a photoresist film pattern, on the second interlayer insulation layer, in  
15          the form of laterally spaced apart stripes of photoresist extending parallel to the gate  
16          stacks, the photoresist film pattern exposing segments of the bit line stacks and  
17          exposing portions of the second interlayer insulation layer located directly above  
18          respective ones of the conductive film pads, respectively;  
19          etching the second interlayer insulation layer and the first interlayer insulation  
20          layer using the photoresist film pattern, the bit line stacks and the bit line spacers as  
21          etching masks to form contact holes exposing the conductive film pads by;  
22          filling the contact holes with a conductive material to form conductive plugs  
23          contacting the conductive film pads;

24 sequentially forming a third interlayer insulation layer, an etch stop layer, an  
25 oxide layer and a hard mask layer on the conductive plugs, the bit line stacks and  
26 the second interlayer insulation layer;

27 forming a second photoresist film pattern on the hard mask layer;

28 etching the hard mask layer and the oxide layer using the second photoresist  
29 film pattern as an etching mask until portions of the etch stop layer are exposed;

30 subsequently removing the second photoresist film pattern; and

31 forming second contact holes for use in forming capacitor lower electrodes by  
32 sequentially removing the exposed etch stop layer and underlying portions of the  
33 third interlayer insulation layer using the hard mask layer as an etching mask, the  
34 second contact holes exposing the conductive plugs.

1 10. The method of claim 9, further comprising the step of filling the second  
2 contact holes with a conductive material to form capacitor lower electrodes  
3 contacting the conductive plugs.

1 11. The method of claim 9, wherein said forming of the gate stacks  
2 comprises sequentially forming a gate insulation layer, a gate conductive layer and a  
3 gate capping layer on the semiconductor substrate.

1 12. The method of claim 9, wherein said forming of the bit line stacks  
2 comprises sequentially forming a barrier metal layer, a bit line conductive layer and a  
3 bit line capping layer on the first interlayer insulation layer.

1       13. The method of claim 9, wherein said forming of the second interlayer  
2 insulation comprises forming a layer of insulating material over the first interlayer  
3 insulation layer and the bit line stacks, and planarizing the layer of insulating  
4 material until upper surfaces of the bit line stacks are exposed.

1       14. The method of claim 13, wherein said planarizing comprises chemical  
2 mechanical polishing.

1       15. The method of claim 9, wherein said forming of the conductive plugs  
2 comprises depositing conductive material sufficient to form a layer that fills the  
3 contact holes and covers the bit line stacks, and planarizing the layer of conductive  
4 material to expose the upper surfaces of the bit line stacks.

1       16. The method of claim 15, wherein said planarizing is performed using  
2 an etch back technique.

1       17. The method of claim 15, wherein said planarizing comprises chemical  
2 mechanical polishing.

1       18. The method of claim 9, wherein the etch stop layer is formed of a  
2 material having an etching selection ratio with respect to the oxide layer.

1       19. The method of claim 18, wherein said forming of the etch stop layer  
2 comprises forming a silicon nitride layer on the third interlayer insulation layer.

1           20. The method of claim 9, wherein the third interlayer insulation layer is  
2 formed of a material having an etching selection ratio with respect to the etch stop  
3 layer.

PCT/US2013/047294 - 10/10